ABSTRACT OF THE DISCLOSURE

A semiconductor memory device having a gate electrode and a diffusion layer, comprising a plurality of memory cells each of which including the gate electrode and the diffusion layers; a first contact layer connected to one of the diffusion layer of the memory cell; a second contact layer connected to the first contact layer; a bit line connected to the second contact layer; and a conductive layer connected to at least two of the diffusion layers that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being same as a height of the first contact layer.